AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Fig. [lsp1]. This sheet, which includes Fig. [lsp2], replaces the original sheet including Fig. [lsp3]. In Figure [lsp4], [lsp5]previously omitted element ___ has been added.

Attachment: Replacement Sheet(s)
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Claims 1, 3 and 6-32 stand in the present application, claims 3, 8 and 31 having been amended. Reconsideration and favorable action is respectfully requested in view of the above amendments and the following remarks.

In the Office Action, the Examiner has objected to claims 3, 8 and 31 for a number of technical deficiencies. As noted above, Applicants have amended each of these claims in accordance with the Examiner's helpful comments. Accordingly, the Examiner's objection to the claims is believed to have been overcome.

The Examiner has rejected claims 1, 3, 6-7, 11-22 and 26-31 under 35 U.S.C. § 103(a) as being unpatentable over Ohno et al. (hereinafter "Ohno") in view of Sekiguchi et al. (hereinafter "Sekiguchi"); has rejected claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Ohno and Sekiguchi and further in view of Blanset et al. (hereinafter "Blanset"); has rejected claims 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Ohno and Sekiguchi in view of Endo et al. (hereinafter "Endo"); and has rejected claim 32 under 35 U.S.C. § 103(a) as being unpatentable over Ohno and Sekiguchi and further in view of Cota-Robles. Applicants respectfully traverse the Examiner's § 103 rejections of the claims.

The last two features of independent claims 1 and 30 require:

> wherein switching between said operating systems includes invoking the common program by calling an exception vector, and
>
> wherein calling an exception vector to invoke the common program simulates an exception caused by an external event.

The Examiner has acknowledged that the feature of "calling an exception vector to invoke the common program simulates an exception caused by an external event" is not disclosed in Ohno, but relies on Sekiguchi for this teaching citing in particular paragraphs [0057], [0072] and [0158]. However, it is respectfully submitted that Sekiguchi also does not teach or suggest this feature of Applicants' inventions.

First, it is instructive to note that nowhere in the cited paragraphs does Sekiguchi even refer to an "exception vector" let alone "wherein calling an exception vector to invoke the common program simulates an exception caused by an external event." Indeed, the cited paragraphs do not even describe simulating anything.

To the contrary, the cited paragraphs of Sekiguchi disclose that when an interrupt occurs, an interrupt controller 101 transmits an interrupt number to the processor 101. The interrupt number is used to acquire an interrupt handler address from an interrupt table 107. The interrupt table 107 is contained in a common area 123 in the main memory 102 shared by first and second OSs. The processor passes control to the interrupt handler address and starts an interrupt management program 204. This involves using an interrupt identification (discrimination) table 1520 that indicates which OS processes an interrupt.

Paragraph [0158] also discloses that the interrupt handler 107 captures external interrupts. The interrupt handler then identifies which OS and which interrupt handler processes this interrupt. Control is then passed to the identified interrupt handler (see also Fig. 15). Applicants respectfully submit that the described operation of Sekiguchi is not relevant to the presently claimed inventions since it has nothing to do with first and

second OSs simulating an external event by calling exception vectors, thereby to invoke a common program, as required by the present claims.

The Examiner appears to argue that using a "virtual" address when processing an exception caused by an external event is the same as "simulating" the external interrupt (see, office action page 3, last paragraph). Clearly this is incorrect. "Simulating" an exception caused by an external event means "imitating" such an exception, without a "real" such exception being necessary or required.

Sekiguchi's use of "virtual" address mapping has no bearing on the actual exception or the corresponding event. Using virtual address mapping does not make the exception or event "unhappen." The exception is still a real exception caused by a real external event, regardless of how the exception is subsequently processed. In other words, a real event does not turn into a "simulated" (imitated) event, as required by the present claims, simply because virtual address mapping is used after the real event has taken place.

Even if using "virtual" addresses is similar to simulating real addresses, which *arguendo* will be taken to be the case, this is not what the claimed invention requires. The claimed invention is not concerned with simulating addresses, but with simulating exceptions caused by external events, as clearly expressed in the present claims.

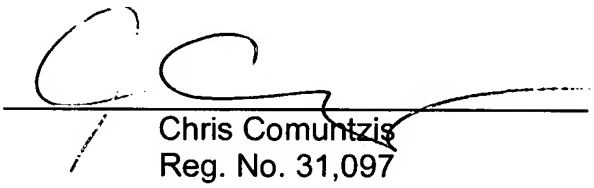
Accordingly, independent claims 1 and 30 and their respective dependent claims are believed to patentably define over Ohno and Sekiguchi taken singly or in combination. Moreover, since it should be clear that the secondary references of Blanset, Endo, and Cota-Robles do not solve the deficiencies described above of Ohno

and Sekiguchi it is respectfully submitted that the present claims patentably define over all of the cited prior art taken singly or in any combination.

Therefore, in view of the above amendments and remarks, it is respectfully requested that the application be reconsidered and that all of claims 1, 3 and 6-32, standing in the application, be allowed and that the case be passed to issue. If there are any other issues remaining which the Examiner believes could be resolved through either a supplemental response or an Examiner's amendment, the Examiner is respectfully requested to contact the undersigned at the local telephone exchange indicated below.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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